CS 223

SECTION 3

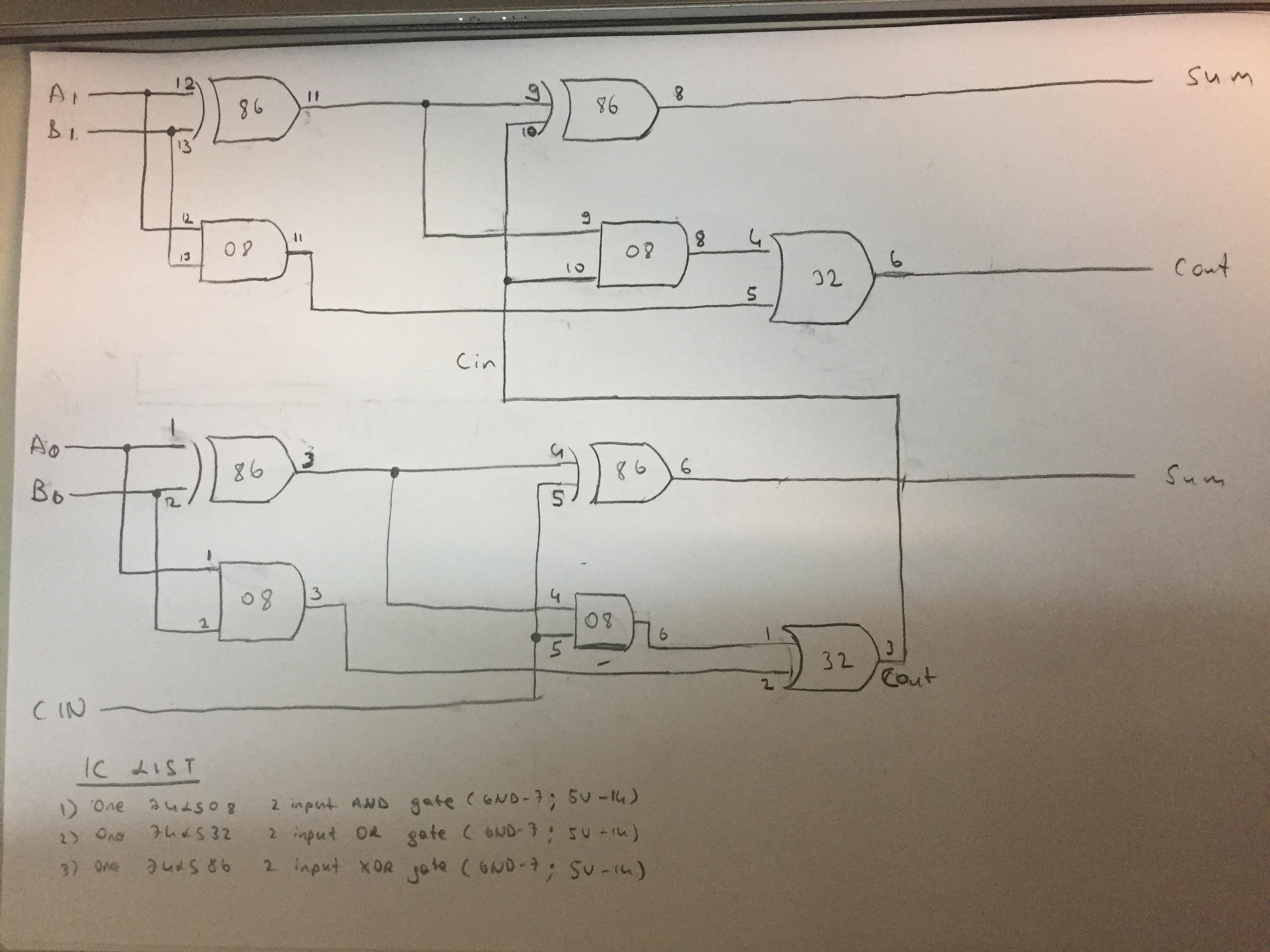
BERAT BİÇER

21503050

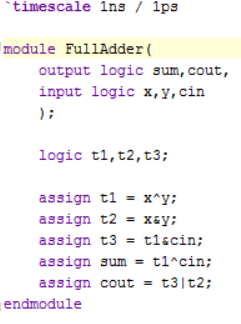
24.10.2016

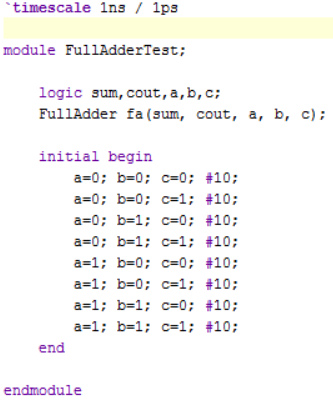
BOX 7

2-BIT ADDER SCHEMATIC



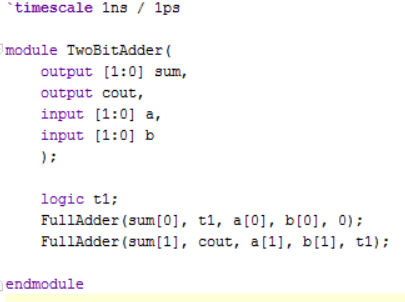
VERILOG MODULE & TESTBENCH FOR A FULL-ADDER





VERILOG MODULE & TESTBENCH FOR A TWO BIT ADDER

Code:



Test Bench:

